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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
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EXAMINER	
KENNEDY, JENNIFER M	

ART UNIT	PAPER NUMBER
2812	

DATE MAILED: 01/05/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/849,311	HONG ET AL.	
	Examiner	Art Unit	
	Jennifer M. Kennedy	2812	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *25 October 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-34* is/are pending in the application.

4a) Of the above claim(s) *25-34* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-24* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *8/11/04*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Election/Restrictions

Applicant's election with traverse of claims 1-24 in the reply filed on October 25, 2004 is acknowledged. The traversal is on the ground(s) that the inventions are so closely related to each other that they would not be a serious burden for the Examiner to examine all of the claims at one time. This is not found persuasive.

A restriction requirement between one set of process claims and a set of product claims was issued in the Office action mailed September 30, 2004. "Section 121 [of Title 35 USC] permits a restriction for 'independent and distinct inventions,' which the PTO construes to mean that the sets of claims must be drawn to separately patentable inventions." See *Applied Materials Inc. v. Advanced Semiconductor Materials* 40 USPQ2d 1481, 1492 (Fed. Cir 1996)(Archer, C.J., concurring in-part and dissenting in-part). A product and the process of making the product are "two independent, albeit related inventions." See *In re Taylor*, 149 USPQ 615, 617 (CCPA 1966). "When two sets of claims filed in the same application are patentably distinct or represent independent inventions, the examiner is to issue a restriction requirement." See *In re Berg*, 46 USPQ2d 1226, 1233 n.10 (Fed. Cir. 1998).

The examiner, in issuing a restriction requirement, must demonstrate "one way distinctiveness." *Applied Materials Inc.* at 1492. As stated within the restriction requirement, "inventions are distinct if either or both of the following can be shown: (1) that the process as claimed can be used to make other and materially different product or (2) that the product as claimed can be made by another and materially different

process (MPEP § 806.05(f))." In this application, the examiner restricted the product claims from the process claims on the grounds that the product as claimed can be made by another and materially different process such as a process such as etching back without the step of performing CMP, and that, as a result, a restriction was necessary.

In addition to one way distinctiveness, the examiner must show "why it would be a burden to examine both sets of claims." *Applied Materials Inc.* at 1492. "A serious burden on the examiner may be *prima facie* shown if the examiner shows by appropriate explanation either separate classification, separate status in the art, or a different field of search." MPEP 803. An explanation was provided in the restriction requirement. Specifically, in addition to being distinct, the examiner indicated that restriction is proper because the product claims and the process claims "have acquired a separate status in the art."

The criteria of distinctness and burdensomeness have been met, as demonstrated hereinabove. Accordingly, the restriction requirement in this application is still deemed proper and is therefore made FINAL.

Claims 25-34 are withdrawn from further consideration pursuant to 37 CFR 1.142(b), as being drawn to a nonelected invention, there being no allowable generic or linking claim. Applicant timely traversed the restriction (election) requirement in the reply filed on October 25, 2004.

Claim Objections

Claims 8 and 22 are objected to because of the following informalities: The claim recites "wherein the etch back step is comprised of an overetch portion". The etching step is a method and cannot be comprised of any material or portion. The examiner believes that this limitation contains a typographical error and that applicant intended to recite "wherein the etch back step creates an overetched portion". Appropriate correction is required.

Claim Rejections - 35 USC § 103

Claims 1-4, 6-12, 15-16, 18-24 are rejected under 35 U.S.C. 103(a) as being unpatentable over Applicants admitted prior art ("AAPA" see specification, pages 1-5 and Figures 1-4) in view of Huang et al. (U.S. Patent No. 5,747,382) and Park (U.S. Patent No. 6,025,223).

In re claim 1, AAPA disclose the method for planarizing an MRAM cell structure on an MRAM chip having an insulation layer (5) with an uneven top surface (see Figure 3) formed on an MTJ (4) which is comprised of a bottom layer (10, 11, 12) on a substrate, a free layer (14) on the bottom layer, and a cap layer (15) on the free layer, comprising:

performing a CMP step to planarize said insulation layer (see specification, page 4, lines 1-5).

AAPA does not disclose the method wherein the planarization includes two steps of performing a CMP step to planarize said insulation layer wherein the planarized insulation layer has a certain thickness above said cap layer and performing an etch back step to reduce the thickness of said insulation layer wherein the insulation layer is planarized.

Huang et al. teach the method of performing a CMP step to planarize said insulation layer wherein the planarized insulation layer has a certain thickness above said cap layer and performing an etch back step to reduce the thickness of said insulation layer wherein the insulation layer is planarized (see column 3, line 48 through column 4, line 10).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to planarize by the method of Huang et al. because as Huang et al. teach it prevents the eruption of debris created in voids of high aspect ratio holes (see column 2, lines 18 through 40 and column 4, lines 1-10).

Neither the AAPA nor Huang et al. disclose the method wherein the insulating is planarized at a certain thickness below said cap layer. Park discloses the method wherein the insulating is planarized at a certain thickness below said cap layer (see column 6, lines 15-30 and Figure 9).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to planarize at a certain thickness below the cap layer in order to

ensure that all insulation material is removed form the surface of the layer to allow for subsequent electrical connection.

In re claim 7, the combined AAPA, Huang et al. and Park disclose the method wherein the etch back step is a plasma etch based on a fluorocarbon chemistry that has a high selectivity between the insulation layer and said cap layer (see Huang et al. column 4, lines 1-10).

In re claim 8, the combined AAPA, Huang et al. and Park disclose the method wherein the etch back step is comprised of an overetch portion. Interpreting as broadly as possible Huang et al. teaches the method wherein the etch back step is comprised of an overetch portion (see column 4, lines 1-10). The examiner notes the first step CMP can be considered and etch step and the etch back step can be considered overetching (etching further or more over an already etched location). Further, Park teaches and overetch portion (see column 6, lines 15-30 and Figure 9).

In re claims 2, 3, 4, 9, and 10, the combined AAPA, Huang et al. and Park disclose the method as claimed and rejected above, including the method wherein the insulation layer is comprised of silicon oxide or a low k dielectric material (see AAPA (5)), and wherein the etch back process has an high etching uniformity of +/- 5 % (Huang et al., column 3, lines 18-30).

The combined AAPA, Huang et al. and Park do not disclose the method wherein the insulation layer has a thickness of about 800 to 2000 Angstroms above said cap

layer before said CMP step, wherein the certain thickness above the cap layer is about 60 to 200 Angstroms, wherein said certain thickness below the cap layer is about 50 to 190 Angstroms, wherein the cap layer has a thickness that is reduced by less than 5 Angstroms during said etch back step, wherein said MRAM chip is further comprised of a plurality of MTJs that have a cap layer thickness variation of less than +/- 5 Angstroms after the etch back step, and wherein the cap layer thickness is between about 50 and 400 Angstroms.

The examiner notes that Applicant does not teach that the thickness ranges recited solve any stated problem or are for any particular purpose. Therefore, the recited thickness ranges lack criticality in the claimed invention and do not produce unexpected or novel results. The examiner notes that Applicant has provided only an advantage to having the cap layer thickness variation of less than +/- 5 Angstroms. Huang et al. teaches an etching back step that allows for +/- 5% uniformity, which at the claimed thickness ranges would correspond to approximately +/- 5 Angstroms for some of the range. Thus, it would have been obvious to one of ordinary skill in the art at the time the invention was made to form the layers of recited thicknesses, since the invention would perform equally well when other thickness ranges are utilized, and because it has been held that where the general conditions of a claim are disclosed in the prior art, discovering the optimum or workable ranges involves only routine skill in the art. *In re Aller,* 105 USPQ 233, MPEP 2144.05 II A.

In re claim 11, AAPA discloses a method for fabricating an MRAM cell structure on an MRAM chip, comprising:

forming a first conductive layer (3) comprised of a first line on a substrate;

forming an MTJ (4) on said first line, said MTJ has a bottom layer (10, 11, 12, 13), a free layer (14) on said bottom layer, and a cap layer (15) on said free layer;

depositing an insulation layer (5) on said MTJ and on said substrate;

performing a CMP step to planarize said insulation layer; and

forming a second conductive layer on said insulation layer and cap layer, said second conductive layer is comprised of a second line that contacts the top surface of said cap layer (see specification, page 4, lines 1-5).

AAPA does not disclose the method wherein the planarization includes two steps of performing a CMP step to planarize said insulation layer wherein the planarized insulation layer has a certain thickness above said cap layer and performing an etch back step to reduce the thickness of said insulation layer wherein the insulation layer is planarized.

Huang et al. teach the method of performing a CMP step to planarize said insulation layer wherein the planarized insulation layer has a certain thickness above said cap layer and performing an etch back step to reduce the thickness of said insulation layer wherein the insulation layer is planarized (see column 3, line 48 through column 4, line 10).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to planarize by the method of Huang et al. because as Huang et al. teach it prevents the eruption of debris created in voids of high aspect ratio holes (see column 2, lines 18 through 40 and column 4, lines 1-10).

Neither the AAPA nor Huang et al. disclose the method wherein the insulating is planarized at a certain thickness below said cap layer. Park discloses the method wherein the insulating is planarized at a certain thickness below said cap layer (see column 6, lines 15-30 and Figure 9).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to planarize at a certain thickness below the cap layer in order to ensure that all insulation material is removed form the surface of the layer to allow for subsequent electrical connection.

In re claim 12, the AAPA disclose the method wherein the bottom layer of said MTJ is a composite layer comprised of a seed layer (10) on said first line, an AFM layer on the seed layer (11), a pinned layer on the AFM layer (12), and a tunnel barrier layer on the pinned layer (13).

In re claim 21, the combined AAPA, Huang et al. and Park disclose the method wherein the etch back step is a plasma etch based on a fluorocarbon chemistry that has a high selectivity between the insulation layer and said cap layer (see Huang et al. column 4, lines 1-10).

In re claim 22, the combined AAPA, Huang et al. and Park disclose the method wherein the etch back step is comprised of an overetch portion. Interpreting as broadly as possible Huang et al. teaches the method wherein the etch back step is comprised of an overetch portion (see column 4, lines 1-10). The examiner notes the first step CMP can be considered and etch step and the etch back step can be considered overetching (etching further or more over an already etched location). Further, Park teaches and overetch portion (see column 6, lines 15-30 and Figure 9).

In re claims 15, 16, 18, 19, 20, 23, and 24, the combined AAPA, Huang et al. and Park disclose the method as claimed and rejected above, including the method wherein the insulation layer is comprised of silicon oxide or a low k dielectric material (see AAPA (5)), wherein the etch back process has an high etching uniformity of +/- 5 % (Huang et al., column 3, lines 18-30), and wherein the MRAM chip is further comprised of an array of lines in said first conductive layer that are parallel to said first line, an array of lines in the second conductive layer that are parallel to the second line, and an array of MTJS formed at each location where a second line crosses over a first line (see AAPA, page 1, lines 7-20).

The combined AAPA, Huang et al. and Park do not disclose the method wherein the insulation layer has a thickness of about 800 to 2000 Angstroms above said cap layer before said CMP step, wherein the certain thickness above the cap layer is about 60 to 200 Angstroms, wherein said certain thickness below the cap layer is about 50 to

190 Angstroms, wherein the cap layer has a thickness that is reduced by less than 5 Angstroms during said etch back step, wherein said MRAM chip is further comprised of a plurality of MTJs that have a cap layer thickness variation of less than +/- 5 Angstroms after the etch back step, and wherein the cap layer thickness is between about 50 and 400 Angstroms, wherein the MTJ has a width from about 0.2 to 0.9 microns, and wherein the distance between a free layer and an overlying second line is maintained to within 10 Angstroms.

The examiner notes that Applicant does not teach that the thickness ranges recited solve any stated problem or are for any particular purpose. Therefore, the recited thickness ranges lack criticality in the claimed invention and do not produce unexpected or novel results. The examiner notes that Applicant has provided only an advantage to having the cap layer thickness variation of less than +/- 5 Angstroms. Huang et al. teaches an etching back step that allows for +/- 5% uniformity, which at the claimed thickness ranges would correspond to approximately +/- 5 Angstroms for some of the range. Thus, it would have been obvious to one of ordinary skill in the art at the time the invention was made to form the layers of recited thicknesses, since the invention would perform equally well when other thickness ranges are utilized, and because it has been held that where the general conditions of a claim are disclosed in the prior art, discovering the optimum or workable ranges involves only routine skill in the art. *In re Aller,* 105 USPQ 233, MPEP 2144.05 II A.

Claims 5 and 17 are rejected under 35 U.S.C. 103(a) as being unpatentable over Applicants admitted prior art ("AAPA" see specification, pages 1-5 and Figures 1-4), Huang et al. (U.S. Patent No. 5,747,382) and Park (U.S. Patent No. 6,025,223) in view of Katti (U.S. Patent Appl. 2003/0146459).

In re claim 5 and 17, the combined AAPA, Huang et al. and Park disclose the method as claimed, and rejected above, but do not disclose the method wherein the cap layer is comprised of Cu, Ru, or a composite layer with an upper Ru layer. Katti discloses the method wherein the cap layer is formed of copper (416). It would have been obvious to one of ordinary skill in the art at the time the invention was made to form the cap layer of copper because, as Katti et al. teach, copper allows for adhesion and a barrier to diffusion (see 0044]). Further, Katti et al. teach that copper is interchangeable with the AAPA tantalum cap layer and, therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to utilize copper in place of the tantalum since it has been held that the selection of a known material based on its suitability for its intended use supported a prima facie obviousness determination in Sinclair & Carroll Co. v. Interchemical Corp., 325 U.S. 327, 65 USPQ 297 (1945). See also In re Leshin, 227 F.2d 197, 125 USPQ 416 (CCPA 1960).

Claims 13 and 14 are rejected under 35 U.S.C. 103(a) as being unpatentable over Applicants admitted prior art ("AAPA" see specification, pages 1-5 and Figures 1-

4), Huang et al. (U.S. Patent No. 5,747,382) and Park (U.S. Patent No. 6,025,223) in view of Hineman et al. (U.S. Patent No. 6,783,995).

In re claim 13 and 14, the combined AAPA, Huang et al. and Park disclose the method as claimed, and rejected above, but do not disclose the method wherein the first line is comprised of copper, and wherein the second line is comprised of copper. Hineman et al. disclose the method wherein the interconnections are formed of copper (see column 1, line 65 through column 2, line 11). It would have been obvious to one of ordinary skill in the art at the time the invention was made to form the bitline and the wordline of the AAPA with copper because, as Hineman et al. teach, copper reduces the likelihood of problems with electromigration caused by the high current density carried by the bit and word lines, and since it has been held that the selection of a known material based on its suitability for its intended use supported a prima facie obviousness determination in Sinclair & Carroll Co. v. Interchemical Corp., 325 U.S. 327, 65 USPQ 297 (1945). See also In re Leshin, 227 F.2d 197, 125 USPQ 416 (CCPA 1960).

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Jennifer M. Kennedy whose telephone number is (571) 272-1672. The examiner can normally be reached on Mon.-Fri. 8:30-5:00.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, John Niebling can be reached on (571) 272-1679. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Jennifer M. Kennedy
Patent Examiner
Art Unit 2812

jmk